REMARKS

In accordance with the foregoing, claims 49 and 73 have been amended and claim 56 has been cancelled, without prejudice or disclaimer. No new matter is being presented, and approval and entry are respectfully requested. Claims 62, 64, 85, and 87 stand in condition for allowance.

Claims 49-55 and 57-94 are pending and under consideration. Reconsideration is requested.

Foreign Priority:

In the Amendment filed on June 12, 2003, the Applicant's representative indicated that the Examiner has not yet acknowledged the Applicant's claim for foreign priority and submission of a certified copy of the **foreign priority document filed on March 21, 2000**. The Applicant respectfully requests that the Examiner acknowledge the same.

In response, on page 2 of the present Office Action, the Examiner has requested the PTO-1449 form for the IDS filed on March 21, 2000. Applicant did not file an IDS on March 21, 2000, but on March 20, 2000, which already has been acknowledged.

Applicant is respectfully requesting that the foreign priority, not an IDS, be acknowledged.

CHANGES TO THE ABSTRACT:

The abstract have been reviewed in response to this Office Action. No new matter has been added as there is support for the changes in portions of the specification and drawings as originally filed.

REJECTION UNDER 35 U.S.C. § 112:

In the Office Action, at pages 2-3, claims 49-61, 63, 65-84, 86, and 88-94 are rejected under 35 U.S.C. § 112, second paragraph, for indefiniteness.

In response, the claims have been amended to improve clarity.

Accordingly, it is respectfully requested that the § 112, second paragraph rejections to the claims be withdrawn.

REJECTION UNDER 35 U.S.C. § 102:

In the Office Action, at pages 3, claims 49-55, 57-61, 63, 65-84, 86, and 88-94 are rejected under 35 U.S.C. § 102 in view of U.S. Patent No. 5,875,324 to Tran et al. ("Tran"). This rejection is traversed and reconsideration is requested.

Tran is limited to a branch prediction unit that is configured to delay updating the branch prediction array until a first clock cycle in which the fetch address is inhibited (other claims are the dependent claims thereof). Therefore, Tran provides that writing cannot inherently interfere with array reading by a fetch request.

In contrast, independent claim 49 recites, "a control unit controlling the memory unit and the branch prediction unit in such a way that **writing of branch history information** in the branch prediction unit **and control** over **fetching of the instruction string** in the memory unit **may not occur simultaneously**." Emphasis added. Tran limits its description to provide **new prediction information** to update the branch prediction array in the clock cycle **following** the cycle in which the **correct address is fetched**.

Further, an update in Tran is delayed until a cycle in which the current fetch PC register is valid. See column 2, lines 24-26, and column 10, lines 40-42. However, Tran is silent as to teaching or suggesting, "a counter to count several clock cycles (several states) **to delay**, for a period of several clock cycles (several states), the **writing** of the branch history information and control, **beforehand**, the **fetching** of the instruction string," emphasis added, as recited in independent claim 49. Tran limits its description to providing a branch update data register 256 storing branch counters in branch holding register 250. The successor index includes the index bits for instruction cache 204 of the branch prediction for the branch instruction. The branch counters are counters associated with the branch prediction mechanisms employed by microprocessor 200. The recitations of independent claim 49 are not anticipated by the cited reference.

Regarding item (e), page 4 of the Office Action, a "pre-fetch" is one of the instructions that can be issued, even at a time in which a requested side cannot issue an instruction of an expected kind due to a cause leading to an inter-lock, for example, due to a resource shortage such as the cue being full or the I-buffer being full, because the instructions are irrelevant to the

cause of the inter-lock (not affected by and not affecting the cause of the inter-lock). The "pre-fetch" of the present claims is not provided in Tran.

Regarding item (h) on page 5 of the Office Action, a temporary instruction buffer is not an instruction cache, contrary to the contentions made in the Office Action. A cache, in general, stores a set of data or the like that is used again at a later time. In contrast, a temporary instruction buffer is a queue and functions as a buffer to buffer between a instruction executing unit and an instruction cache. "If the temporary instruction buffer unit is empty" indicates that the supply of instructions is short and, therefore, an instruction fetch request is given a priority.

Further, in Tran, if update information that is presented for update matches a fetch request, then the update is bypassed and prediction information is forwarded, because the presented update information is just subsequent prediction information. A register file timing diagram is illustrated in FIG. 37 of Tran. See column 162, lines 10-31.

However, nothing in Tran teaches or suggests, "a bypass unit making the branch history information of the branch instruction a research target of a branch prediction," as recited in claim 70. Nowhere in FIG. 37 and FIG. 46 of Tran is there a teaching or suggestion of the recitations of the bypass unit recited in independent claim 49. Rather, Tran provides sixteen 5-bit comparators, which detect if forwarding is needed from a writeback port to a read port. The forwarding will bypass the delay through the register latch and help allow the read to complete within the cycle. Further, for null segment indications from microcode and when all the segment bases are zero, there is a bypass path to the load-store buffer from the functional units. See column 169, lines 55-60.

Because independent claim 73 includes similar claim features as those recited in independent claim 49, although of different scope, and because the Office Action refers to similar portions of the cited references to reject independent claim 73, the arguments presented above supporting the patentability of independent claim 49 are incorporated herein to support the patentability of independent claim 73.

Accordingly, it is respectfully asserted that the recitations of independent claims 49 and 73 are not taught or suggested by Tran. It is respectfully requested that independent claims 49 and 73 and related dependent claims be allowed.

CONCLUSION:

In accordance with the foregoing, it is respectfully submitted that all outstanding objections and rejections have been overcome and/or rendered moot, and further, that all pending claims patentably distinguish over the prior art. There being no further outstanding objections or rejections, the application is submitted as being in condition for allowance, which action is earnestly solicited.

If the Examiner has any remaining issues to be addressed, it is believed that prosecution can be expedited by the Examiner's contacting the undersigned attorney for a telephone interview to discuss resolution of such issues.

If there are any underpayments or overpayments of fees associated with the filing of this Amendment, please charge and/or credit the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

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By: _____
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